CLAIMS

We claim:

1. A method for obtaining an output signal from a light sensing circuit wherein operation of the light sensing circuit includes a reset phase during which a photo sensing node of the light sensing circuit is charged to a reference voltage and an integration phase during which voltage at the photo sensing node is modified by a photocurrent according to incident light intensity, the method comprising:

correlated double sampling of the photo sensing node voltage to obtain an output signal representative of a change in voltage at the photo sensing node over the time of said integration phase; and

holding said output signal for processing;

wherein the correlated double sampling comprises following the photo sensing node voltage from a first time instant occurring after completion of a said integration phase and before instigation of a subsequent said reset phase, to a second time instant occurring after completion of said subsequent reset phase.

2. A method as claimed in claim 1, wherein said reset phase comprises charging said photo sensing node to said reference voltage by turning on and off a reset transistor coupled to the photo sensing node such that, after turning off the reset transistor, a feed through effect at the reset transistor causes a reduction in voltage at the photo sensing node before instigation of the subsequent reset phase, and wherein the second time instant of said correlated double sampling is after said photo sensing node voltage reduction due to feed through effect.

3. A method as claimed in claim 1, wherein a sample and hold circuit is coupled receive signals representing the photo sensing node voltage, and a clamping circuit is coupled to the sample and hold circuit, and wherein said correlated double sampling and said holding of the output signal is accomplished by manipulation of input signals to said sample and hold circuit and said clamping circuit.

4. A method as claimed in claim 1, wherein said light sensing circuit includes a photo-diode coupled to said photo sensing node, and wherein said photo-current flows through the photo-diode according to the intensity of light incident thereon.

5. A method as claimed in claim 1, wherein said light sensing circuit includes a photo-gate transistor coupled to said photo sensing node and through which said photo-current flows according to the intensity of light incident thereon.

6. A method as claimed in claim 1, wherein said integration phase and said reset phase are performed in an alternating cycle, and wherein an output signal is obtained for said light sensing circuit following each cycle.

7. A method as claimed in claim 6, wherein a plurality of said light sensing circuits are arranged in a two dimensional image sensing array, and wherein an output signal is obtained for each of said light sensing elements in the array following each said cycle, so as to obtain two dimensional image data.

8. A method as claimed in claim 7, wherein a sample and hold circuit is coupled to selectively receive signals representing the photo sensing node voltage from a plurality of light sensing circuits in said array, and a clamping circuit is coupled to the sample and hold circuit, and wherein said correlated double sampling and said holding of the output signal is accomplished by manipulation of input signals to said sample and hold circuit and said clamping circuit.

9. A method as claimed in claim 3, wherein said light sensing circuit, said sample and hold circuit and said clamping circuit are all fabricated on the same silicon substrate using a CMOS integrated circuit technology.

10. A sampling circuit for an image sensing circuit having a photosensitive element which develops a photo sensing node voltage according to incident light, the sampling circuit comprising:

an amplifier circuit having said photo sensing node voltage as input;

a sample and hold circuit coupled to receive an output of the amplifier circuit, and a clamping circuit coupled to receive an output of the sample and hold circuit and produce an output signal representing a double correlated sample voltage difference at said photo sensing node.

11. A sampling circuit as claimed in claim 10, wherein the amplifier circuit comprises a differential input transistor pair circuit.

12. A sampling circuit as claimed in claim **10**, wherein the amplifier circuit comprises a source follower circuit.

13. A sampling circuit as claimed in claim **11**, wherein the amplifier circuit has a feedback loop and wherein said sample and hold circuit is coupled within said feedback loop.

14. A sampling circuit as claimed in claim **13**, wherein a source follower circuit coupled within said feedback loop is used to couple the output of the sample and hold circuit to said clamping circuit.

15. A sampling circuit as claimed in claim **14**, wherein said clamping circuit comprises an auto-zero amplifier circuit having a feedback loop which includes a first capacitive storage element coupled in parallel with a switching element controlled by a clamp signal.

16. A sampling circuit as claimed in claim **15**, wherein the amplifier circuit of the clamping circuit has a first input coupled to a reference voltage and a second input coupled by way of a second capacitive element to said sample and hold circuit output, and wherein said clamping circuit is controlled by said clamp signal such that in a first state the output of the clamping circuit amplifier is fixed by said reference voltage and in a second state the clamping circuit output changes in accordance with said

sample and hold circuit output from a baseline of the fixed reference voltage output.

17. A sampling circuit as claimed in claim **13**, wherein a plurality of image sensing circuits are arranged in an array, each forming a pixel circuit of an image sensor, and wherein each pixel circuit includes a said photo sensitive element, a reset switching element and a said differential input transistor pair as part of said amplifier circuit, and wherein the sample and hold circuit and the clamping circuit are shared by a plurality of pixel circuits in the image sensor array.

18. A sampling circuit as claimed in claim **14**, wherein the feedback to the differential input transistor pair is arranged so that the amplifier circuit has a gain of greater than unity.

19. A sampling circuit as claimed in claim **10**, wherein the image sensing circuit, amplifier circuit, sample and hold circuit and clamping circuit are constructed in the same integrated circuit using CMOS fabrication technology.

20. An image sensor circuit having a two dimensional array of light sensitive pixel circuits, each pixel circuit comprising a photosensitive element and a reset switching element coupled to a light sensing node, a differential input transistor pair having a first input thereof coupled to said light sensing node, and an enable switching element coupled to selectively block output from the differential input transistor pair, the

image sensing circuit further comprising sampling circuitry for producing output signals corresponding to light incident on each of the respective pixel circuits.

21. An image sensor circuit as claimed in claim **20**, wherein said sampling circuitry provides a feedback path to a second input of said differential input transistor pair of each of said pixel circuits.

22. An image sensor circuit as claimed in claim **21**, wherein said sampling circuitry includes a sample and hold circuit coupled within said feedback path.

23. An image sensor circuit as claimed in claim **22**, wherein said sampling circuitry further includes a source follower circuit coupled within said feedback path which provides an input to a clamping circuit.

24. An image sensor circuit as claimed in claim **23**, wherein said clamping circuit comprises an auto-zero amplifier circuit.

25. An image sensor circuit as claimed in claim **23**, wherein clamping circuit comprises an auto-zero amplifier circuit having a feedback loop which includes a first capacitive storage element coupled in parallel with a switching element controlled by a clamp signal, and wherein the differential amplifier circuit of the clamping circuit has a first input coupled to a reference voltage and a second input coupled by way of a second capacitive element to receive input from said sample and hold circuit, and wherein said

clamping circuit is controllable by said clamp signal such that in a first state the output of the clamping circuit differential amplifier is fixed by said reference voltage and in a second state the clamping circuit output changes in accordance with the input received from said sample and hold circuit from a baseline of said fixed reference voltage output.

26. An image sensor circuit as claimed in claim **20**, wherein the image sensor array is implemented with CMOS technology.

27. An image sensor array as claimed in claim **20**, wherein the photosensitive element comprises a photo-diode.

28. An image sensor array as claimed in claim **20**, wherein the photosensitive element comprises a photo-gate transistor.

29. In an image sensor circuit having an array of pixels including light sensing nodes at each of which a change in voltage can be imparted by exposure to a light source, a method for obtaining output signals representing the voltage changes at the light sensing nodes in order to obtain image data, comprising:

at each said pixel providing an amplifier circuit with an input driven by the voltage on the respective light sensing node to produce an amplifier output;

providing a sample and hold circuit coupled to selectively receive the amplifier output of a said pixel amplifier circuit in the array, the sample and hold circuit being controlled by a *SAMP* control signal input and producing an output signal;

providing a clamping circuit coupled to receive the sample and hold circuit output, the clamping circuit producing an output according to the received sample and hold signal input and a control signal CLAMP; and

controlling the SAMP and CLAMP control signals to the sample and hold circuit and the clamping circuit respectively so as to perform correlated double sampling of the voltage at the respective light sensing node so as to obtain a representation of the change of voltage thereat imparted substantially only by exposure to light.

30. A sampling circuit for an image sensing circuit having a photosensitive element which develops a photo sensing node voltage according to incident light, the sampling circuit comprising:

a feedback loop amplifier circuit having said photo sensing node voltage as input; and

a clamping circuit coupled to receive an output from the feedback loop amplifier circuit and produce an output signal representing a double correlated sample voltage difference at said photo sensing node.

31. A sampling circuit as claimed in claim **30**, wherein the amplifier circuit includes a source follower circuit coupled within the feedback loop thereof, the source follower circuit supplying output to the clamping circuit.

32. A sampling circuit as claimed in claim **30**, wherein said clamping circuit comprises an auto-zero amplifier circuit.

33. A sampling circuit as claimed in claim **32**, wherein the auto-zero amplifier circuit has a feedback loop which includes a first capacitive storage element coupled in parallel with a switching element controlled by a clamp signal.

34. A sampling circuit as claimed in claim **33**, wherein the amplifier circuit of the clamping circuit has a first input coupled to a reference voltage and a second input coupled by way of a second capacitive element to receive said output from the feedback loop amplifier, and wherein said clamping circuit is controlled by a clamp signal such that in a first state the output of the clamping circuit amplifier is fixed by said reference voltage and in a second state the clamping circuit output changes in accordance with said feedback loop amplifier output from a baseline of the fixed reference voltage output.

35. A sampling circuit as claimed in claim **31**, wherein the feedback of said feedback loop amplifier is arranged so that the amplifier circuit has a gain of greater than unity.

36. A sampling circuit as claimed in claim **30**, further including a sample and hold circuit coupled between the feedback loop amplifier circuit and the clamping circuit.